WHAT IS CLAIMED IS:

1. A read/program potential generating circuit comprising:

a first potential generating circuit that generates a program potential necessary for programming for a fuse element; and

a second potential generating circuit that generates a read potential necessary for checking a state of the fuse element,

wherein a value of the read potential is lower than a value of the program potential.

2. The read/program potential generating circuit according to claim 1, wherein the fuse element is programmed by fusion cutting or dielectric breakdown.

3. A semiconductor device comprising the read/program potential generating circuit according to claim 1 and an external terminal for taking in the program potential.

4. A semiconductor device comprising the read/program potential generating circuit according to claim 1 and a logic circuit driven by a logic power supply potential, wherein the read potential is generated from the logic power supply potential.

5. The read/program potential generating circuit according to claim 1, wherein the programming is executable before or after an assembly step.

6. The read/program potential generating circuit

according to claim 1, wherein the programming is executed based on a command from a CPU.

7. The read/program potential generating circuit according to claim 6, wherein the first potential generating circuit is rendered operative by a program signal produced based on the command, and the second potential generating circuit is rendered operative by Power-On and rendered inoperative by completion of fuse data latch.

8. The read/program potential generating circuit according to claim 7, wherein the second potential generating circuit includes a transistor in an output section thereof, and a drain of the transistor is charged before the second potential generating circuit is rendered inoperative by completion of fuse data latch.

9. The read/program potential generating circuit according to claim 7, wherein the second potential generating circuit includes a transistor in an output section thereof, and a gate of the transistor is charged upon reception of the program signal.

10. The read/program potential generating circuit according to claim 1, wherein the checking is executed in sync with Power-On.

11. A fuse circuit comprising:

the read/program potential generating circuit according to claim 1;

a node commonly connected to the first and second potential generating circuits;

a fuse element having one end connected to the node; and

a barrier transistor connected to the other end of the fuse element.

12. The fuse circuit according to claim 11, wherein the node is set at a ground potential when the program potential is not generated and the read potential is not generated.

13. The fuse circuit according to claim 11, wherein a gate of the barrier transistor is charged when one of the program potential and the read potential is generated.

14. The fuse circuit according to claim 11, wherein one of a chip ID, a security code, and data relating to contrast of a liquid crystal display of a mobile phone, is programmed in the fuse element.

15. A read/program method comprising:

generating a read potential in sync with Power-On;

applying the read potential to a fuse element, thereby checking a state of the fuse element;

generating a program potential higher than the read potential, based on a command from a CPU; and

applying the program potential to the fuse element, thereby executing programming for the fuse element.

16. The read/program method according to claim 15, wherein a ground potential is applied to the fuse element when none of the read potential and the program potential is applied to the fuse element.

17. The read/program method according to claim 15, wherein the application of the read potential to the fuse element is finished when data in the fuse element is latched in a latch circuit.

18. The read/program method according to claim 15, wherein the programming is executable before or after an assembly step.